

United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/803,747	03/17/2004	Lawrence C. Gunn III	LUX-P027	6870	
75	590 02/15/2006		EXAM	INER	
Fernandez & Associates, LLP PO BOX D			BLEVINS,	BLEVINS, JERRY M	
	A 94026-6402		ART UNIT	PAPER NUMBER	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/803,747	GUNN ET AL.	(m)			
Office Action Summary	Examiner	Art Unit				
	Jerry Martin Blevins	2883				
The MAILING DATE of this communication app Period for Reply	pears on the cover sheet with the o	orrespondence address	;			
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DARWING STATE OF THE MAILING DARWING STATE OF THE MAILING DAWNING STATE OF THE MAILING DAWNING STATE OF THE MAILING DAWNING STATE OF THE MAILING STATE OF THE MAILI	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tir will apply and will expire SIX (6) MONTHS from , cause the application to become ABANDONE	N. mely filed the mailing date of this communi ED (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on 19 Ja	anuary 2006.					
2a) ☐ This action is FINAL . 2b) ☑ This	action is non-final.					
·	3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under E	Ex parte Quayle, 1935 C.D. 11, 4	53 O.G. 213.				
Disposition of Claims						
4) ⊠ Claim(s) 1-30 is/are pending in the application. 4a) Of the above claim(s) 17-30 is/are withdray 5) □ Claim(s) is/are allowed. 6) ⊠ Claim(s) 1-16 is/are rejected. 7) □ Claim(s) is/are objected to. 8) □ Claim(s) are subject to restriction and/o	vn from consideration.					
Application Papers	·					
9) The specification is objected to by the Examine	er.					
10)⊠ The drawing(s) filed on <u>17 March 2004</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.						
Applicant may not request that any objection to the	drawing(s) be held in abeyance. Se	e 37 CFR 1.85(a).				
Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the Ex						
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority application from the International Bureau * See the attached detailed Office action for a list	s have been received. s have been received in Applicat rity documents have been receiv u (PCT Rule 17.2(a)).	ion No ed in this National Stag	e			
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail D 5) Notice of Informal I 6) Other:		ı			

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Invention 1 in the reply filed on 01/19/2006 is acknowledged.

Claim Objections

Claim 13 is objected to because of the following informalities:

Claim 13 depends from claim 12, which limits the waveguides to the group: strip loaded waveguides, channel waveguides, rib waveguides, and ridge waveguides.

Claim 12 does not, however, limit the waveguides to any one particular set of waveguides from the group. Claim 13 refers to the "strip loaded waveguide" of claim 12, but this reference lacks antecedent basis, since claim 12 does not limit the waveguides to the particular set of "strip loaded waveguides." For purposes of examination, examiner interprets claim 13 to read "... wherein the waveguide ...".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

⁽b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2883

Claims 1, 2, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by non-patent literature to Yamada et al., "Crosstalk Reduction in a 10-GHz Spacing Arrayed-Waveguide Grating by Phase-Error Compensation", *Journal of Lightwave Technology*, Vol. 16, No. 3.

Regarding claim 1, Yamada teaches an AWG (Figure 1) disposed on a substrate (page 365, last full paragraph) comprising an input slab (slab waveguide directly above input waveguides) with a plurality of inputs and a plurality of outputs (inputs from input waveguides, outputs to arrayed waveguides), an output slab (slab waveguide directly above output waveguides) with a plurality of inputs and a plurality of outputs (outputs to output waveguides, inputs from arrayed waveguides) and a plurality of waveguides (arrayed waveguides) coupled between the input slab and the output slab, where each of the plurality of waveguides has a phase modulator (elements for phase adjustment) in the optical path, and has a predetermined optical path length difference with respect to an adjacent waveguide (page 364, last full paragraph), and wherein each phase modulator has an input for receiving a control signal (from input slab), and the phase modulator modifies the phase of light propagating through it in response to the received control signal (inherent property of phase modulator).

Regarding claim 2, Yamada teaches at least three waveguides coupled between the input slab and the output slab (Figure 1).

Regarding claim 10, Yamada teaches that each of the plurality of waveguides has at least one curved section, where the at least one curved section is substantially identical to a curved section in an adjacent waveguide (Figure 1).

Art Unit: 2883

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of US Pre Grant Publication to Yoo, number 2004/0037500.

Regarding claims 3 and 4, Yamada teaches the limitations of the base claim 3. Yamada does not teach a controller with a first plurality of outputs, where each of the first plurality of outputs is coupled to the control signal input of a respective one of the plurality of phase modulators. Yoo teaches an AWG (Figure 2) comprising a controller (56) with a first plurality of outputs, where each of the plurality of outputs is coupled to the control signal input of a respective one of the plurality of phase modulators (46), comprising a memory system coupled to the controller (page 3, paragraph 35). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yamada with the controller of Yoo. The motivation would have been to improve correction of phase dispersion (page 4, paragraph 41).

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Yoo and further in view of US Pre Grant Publication to Welch et al., number 2004/0033004.

, applications contact that

Art Unit: 2883

Regarding claim 15, Yamada teaches a system for phase error compensation of an AWG (Figure 1) comprising a plurality of phase modulators (elements for phase adjustment), where each phase modulator has an input. Yamada does not teach a controller. You teaches an AWG (Figure 2) comprising a controller (56) with a plurality of inputs and a plurality of outputs, where each of the plurality of outputs is coupled to the input of a respective one of a plurality of phase modulators (46). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yamada with the controller of Yoo. The motivation would have been to improve correction of phase dispersion (page 4, paragraph 41). Yamada also does not teach a plurality of photodetectors. Welch teaches an AWG comprising a controller (RxPIC 10, page 19, paragraph 202) and comprising a plurality of photodetectors (Figure 5, elements 16) where each of the plurality of photodetectors is optically coupled to a respective one of a plurality of outputs of the AWG (Figure 5), and each of the photodetectors has an output coupled to a respective input of the controller (page 19, paragraph 202). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yamada with the photodetectors of Welch. The motivation would have been to improve detection of the phase modulated light.

Regarding claim 16, Yamada teaches a system for phase error compensation of an AWG (Figure 1) comprising a plurality of phase modulators (elements for phase adjustment), where each phase modulator has an input and each phase modulator is in an optical path of a respective one of a plurality of arrayed waveguides of the AWG. Yamada does not teach a controller. Yoo teaches an AWG (Figure 2) comprising a

Art Unit: 2883

controller (56) with an output and an input (not shown) and a plurality of outputs (to modulators 46. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yamada with the controller of Yoo. The motivation would have been to improve correction of phase dispersion (page 4, paragraph 41). Yamada also does not teach a signal generator, a light source, a modulator, a photodetector, and a signal detector. Welch teaches an AWG comprising a controller (RxPIC 10, page 19, paragraph 202, Figures 64, 69, element 10) and comprising a signal generator (Figure 69, element 401) with an input and an output, a light source of a selected frequency (Figure 64, element 302), a modulator (Figure 64, element 306) with an optical input, an optical output and a signal input, a photodetector (Figure 64, element 290) with an optical input and an electrical output, and a signal detector (Figure 64, elements 312, 314, which detect signal from generator 401, Figure 69), where: the output of the controller (10) is coupled to the input of the signal generator (Figure 69), the output of the signal generator is coupled to the signal input of the modulator (Figure 69, where the modulator is part of TxPIC 300, Figure 64), the input of the modulator is coupled to the light source (Figure 64), the output of the modulator is coupled to a selected one of a plurality of inputs to the AWG (Figure 64), the input of the photodetector is coupled to a selected one of a plurality of outputs of the AWG (Figure 64), the output of the photodetector is coupled to the input of the signal detector (Figure 69, where the photodetector is part of RxPIC 10, Figure 64), the output of the signal detector is coupled to the input of the controller (Figure 64, output of 300 coupled to input of controller 10), and each of the plurality of outputs of the controller is coupled to a

Art Unit: 2883

respective one of the plurality of phase modulators (Figure 69, where the modulator is part of element 300). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yamada with the above structures of Welch. The motivation would have been to improve detection of the phase modulated light.

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Yoo as applied to claim 3 above, and further in view of Welch.

Regarding claims 5 and 6, Yamada in view of Yoo teaches the limitations of the base claim 4. Yoo also teaches a first plurality of inputs to the controller (Figure 2). Yamada does not teach a plurality of photodetectors. Welch teaches an AWG comprising a memory system coupled to a controller (RxPIC 10, page 19, paragraph 202) comprising a plurality of photodetectors (Figure 5, elements 16) where each of the plurality of photodetectors has an optical input and an electrical output (inherent to photodetectors), each optical input of the plurality of photodetectors is coupled to a respective one of the plurality of outputs of the output slab (Figure 2), each of the plurality of photodetectors generates an electrical signal at a respective output in response to detected light (inherent to photodetectors) and each output of the plurality of photodetectors is coupled to a respective one of a plurality of inputs to the controller (page 19, paragraph 202), wherein the AWG, the controller, the memory, and the plurality of photodetectors are disposed on a substrate (page 1, paragraph 5, page 8, paragraph 130, and Figure 2). It would have been obvious to one of ordinary skill in the

Art Unit: 2883

art at the time of the invention to modify Yamada with the photodetectors of Welch. The motivation would have been to improve detection of the phase modulated light.

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Yoo and further in view of Welch as applied to claim 5 above, and further in view of US Patent to Koga et al., number 5,617,234.

Regarding claims 7 and 8, Yamada in view of Yoo and further in view of Welch teaches the limitations of the base claim 5. Yamada does not teach a plurality of temperature sensors and a plurality of heating elements. Koga teaches an AWG (Figure 4) comprising a plurality of temperature sensors (Figure 6, element 121, where one sensor corresponds to each of the plurality of waveguides of the AWG 12), where each of the plurality of temperature sensors has an output (coupling to element 21) and each temperature sensor is in substantial thermal proximity to the AWG (Figure 6) and a second plurality of inputs to a controller (temperature control circuit 21, corresponding to outputs of sensor), where each of the second plurality of inputs is coupled to a respective one of the plurality of temperature sensors. Koga also teaches a plurality of heating elements (column 1, lines 41-56, one heater corresponds to each of the plurality of waveguides of the AWG 12), where each of the plurality of heating elements has an input and each of the plurality of heating elements is in substantial proximity to the AWG (column 1, lines 41-56 and Figure 4), and a second plurality of outputs from the controller, where each of the second plurality of outputs is coupled to a respective one of the plurality of heating elements (as shown by the coupling of the control circuit and

Art Unit: 2883

the current circuit, Figure 4). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yamada with the temperature sensors and the heaters of Koga. The motivation would have been to improve the accuracy of the phase modulation due to the thin-film heater of Yamada.

Regarding claim 9, Yamada in view of Yoo, further in view of Welch, and further in view of Koga teaches the limitations of the base claim 8. Yamada in view of Yoo and further in view of Welch also teaches that the AWG, controller, memory system, and plurality of photodetectors are disposed on a substrate (see rejection of claim 6 above). Yamada does not teach that the plurality of temperature sensors and the plurality of heaters are integrally disposed on the substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yamada such that the plurality of temperature sensors and the plurality of heaters are integrally disposed on the substrate, since it has been held that the use of a one piece construction instead of the structure disclosed in the prior art would be merely a matter of obvious engineering choice, In re Larson, 144 USPQ 347. The motivation would have been to reduce the size of the apparatus.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view US Patent to Lu et al., number 6,233,070.

Regarding claim 11, Yamada teaches the limitations of the base claim 1.

Yamada does not teach that the phase modulator is selected from a transistor, a PIN diode, and a resistor. Lu teaches a PIN diode phase modulator (column 1, line 32 –

Art Unit: 2883

column 2, line 53). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yamada with the PIN diode phase modulator of Lu. The motivation would have been to improve the accuracy of the phase modulation (since the modulation is a known function of the applied voltage, Figure 1 and column 2, lines 3-9).

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of US Pre Grant Publication to Rosenflantz et al., number 2005/0065012.

Regarding claims 12 and 13, Yamada teaches the limitations of the base claim

12. Yamada does not teach that the plurality of waveguides is selected from the group comprising: a strip loaded waveguide, a channel waveguide, a rib waveguide, and a ridge waveguide. Rosenflantz teaches a strip loaded waveguide comprising a strip, a slab, and a low index transition layer between the strip and the slab (page 10, paragraph 111). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yamada with the strip loaded waveguide of Rosenflantz. The motivation would have been to reduce manufacturing costs.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of US Pre Grant Publication to Myrick, number 2004/0248381.

Regarding claim 14, Yamada teaches the limitations of the base claim 1.

Yamada also teaches that the substrate is silicon (page 365, last full paragraph).

Art Unit: 2883

Yamada not teach a first layer of monocrystalline silicon, a second layer of dielectric material disposed on the first layer, a third layer of monocrystalline silicon disposed on the second layer, a fourth layer of dielectric material disposed on the third layer, and a fifth layer of monocrystalline silicon disposed on the fourth layer. Myrick teaches a substrate comprising a first layer of monocrystalline silicon, a second layer of dielectric material disposed on the first layer, a third layer of monocrystalline silicon disposed on the second layer, a fourth layer of dielectric material disposed on the third layer, and a fifth layer of monocrystalline silicon disposed on the fourth layer (Figure 3 and page 3, paragraph 35). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yamada with the layered substrate of Myrick. The motivation would have been to improve the precision and controllability of the substrate dimensions (page 1, paragraph 4).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jerry Martin Blevins whose telephone number is 571-272-8581. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank G. Font can be reached on 571-272-2415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number: 10/803,747 Page 12

Art Unit: 2883

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMB

Frank G. Font
Supervisory Patent Examiner
Technology Center 2800